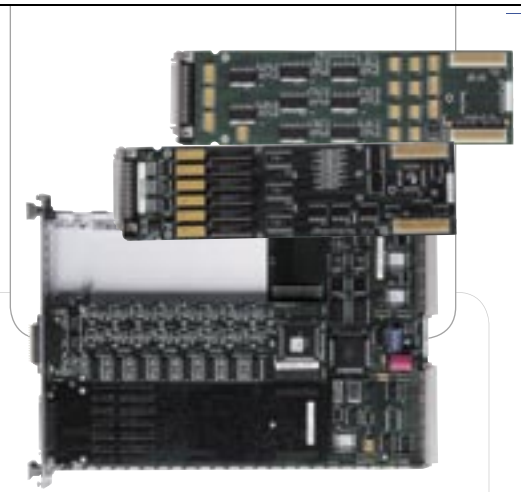

VM1548 48-channel TTL I/O (VMIP™)
VM1548C 48-channel I/O, Open Collector (VMIP™)

Overview

The VM1548 and VM1548C are high-performance I/O modules with six groups of 8 bits (48 channels). Each group of 8 bits may be configured as an input or output under program control or via the front panel control line. The inputs and outputs may be either single buffered to provide real time data access or double buffered to provide synchronized data input and/or output.

The VM1548 and VM1548C belong to the VMIP™ family of products. This gives the user the added flexibility of combining digital I/O with other instruments to create a multi-function C-size card, or with other VM1548s to provide up to 144 I/O channels in a single C-size card slot, the highest density of digital I/O per C-size card.

Features

- Six Groups of 8 I/O Bits Each
- Up to 144 Channels per Single VXIbus C-size Slot
- Message or Register-based Data Access
- ASCII, Hex, Octal, and Binary Data Output Types
- TTL or up to 60 V, 300 mA Open-collector
- Flexible Triggering and Handshaking Capability
- SCPI Compatible
- VXI*plug&play* Drivers

Programming and Data Access

The data may be read or loaded by one of two different methods:

Word Serial Message-based Data Access: In this mode, the input or output data and all other functions are accessed via the VXI message-based interface. Commands are sent to set the I/O ports as well as to initiate functions such as triggering an update or to query a port's input state. This data access method is very clean from a programming perspective, but is also slowest of the data access modes.

Register-based Data Access: This mode offers the fastest throughput. The I/O ports are directly mapped into the VXI user definable registers. Data access occurs in approximately 500 ns, depending on controller and software used.

To further ease programming, VXI*plug&play* drivers are provided.

Flexible Triggering Capability

The VM1548 has the flexibility to source the input and output clocks from either the front panel (one input per group of 8 bits), the backplane TTL trigger bus or via a word serial command. By using the appropriate clocking sources, very large numbers of channels may be synchronized to collect or present data to a UUT.

The ability to source the input and output clocks from the VXIbus TTL trigger lines allows the user to send a trigger to the VXIbus backplane if a certain event is detected. This is done by monitoring one of the six clock inputs, and adds a very useful feature not found in other VXIbus digital I/O cards. By connecting the clock lines to the VXIbus trigger lines and interfacing them to the UUT clock lines, the UUT can handshake between other VXIbus devices, such as the host controller.

VM1548 48-channel TTL I/O (VMIP™)
VM1548C 48-channel I/O, Open Collector (VMIP™)

Specifications

Data Input Characteristics:

VM1548
Vin(high) > 2.0 V
Vin (low) < 0.8 V
Iin (Vin = 2.7 V) < 70 µA
Iin (Vin = 5.0 V) < 1 mA
Iin (Vin = 0.5 V) < -1 mA

VM1548C
Vin(high) > 2.0 V
Vin (low) < 1.5 V
Vin (max) 60 V

Data Output Characteristics:

VM1548
Vout (high) > 2 V** @ -15 mA
Vout (low) < 0.55 V** @ 64 mA
** Voltages are with the damping resistors removed and replaced with shorts

VM1548C
Vout (high) > 2 V - 60 V
Vout (low) < 1.5 volts @ 300 mA

Clock and Control Input Characteristics
Vout(high) > 2.0 V
Vout(low) < 0.8 V
Iin (Vin = 5.0V) < 1 mA, 10 µA VM1548C
Iin (Vin = 0.5V) < -1 mA, 100 µA VM1548C

Data Throughput for 1548:
(Dependent on controller & software)

500 ns typical, direct register access
2 MB per second using D8 access
4 MB per second using D16 access

Data Input Clock Sources:
Front panel, TTL Trigger bus (0-7), word serial event (command). Rising or falling edge

Data Access Types:
Direct register or message-based word serial

Data Output Clock Sources:
Front panel, TTL Trigger bus (0-7), word serial event (command). Rising or falling edge

TTL Trigger Output Sources:
Front panel clock inputs (0-5), Word Serial Event (command). Rising or falling edge

Clocked Input Data Setup:

VM1548	10 ns
VM1548C	2 µs

Clocked Input Data Hold:

VM1548	5 ns
VM1548C	80 ns

User Connector:
The user connector is a standard 68-pin SCSI-2 compatible IDC. A mating connector is provided with each unit

Ordering Information

VM1548	48-channel TTL I/O (must be configured with VM9000 host module)
VM1548C	48-channel Open-collector I/O (must be configured with VM9000 host module)

VM1548/1548C